Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.110”**

**.110”**

**Top Material: Al**

**Backside Material: NiAg**

**Bond Pad Size:B = .021 x .024” E = .024 x .042”**

**Backside Potential: COLLECTOR**

**Mask Ref: CP127**

**APPROVED BY: DK DIE SIZE .110” X .110” DATE: 11/17/21**

**MFG: CENTRAL SEMI THICKNESS .010” P/N: 2N6301**

**DG 10.1.2**

#### Rev B, 7/1